AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listing of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A single crystal oscillator RF transmitter system comprising:

a microprocessor;

a converter coupled to said microprocessor for converting digital data output from the microprocessor into digital packet data to be transmitted ~~into packets~~ by the system;

a local oscillator responsive to an external crystal for generating a first clock signal having a frequency in a radio frequency band;

a clock switch coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter, the third clock signal being a different frequency than the first clock signal and the second clock signal; and

a transmitter connected to an output of the converter for receiving the ~~packets~~ digital packet data and being coupled to the local oscillator for use of the first clock signal as an ~~rf~~ RF carrier for the ~~packets~~ digital packet data to be transmitted by the transmitter;

wherein the microprocessor, converter, local oscillator, clock switch and transmitter are integrated on a chip.

2. (Previously presented) The system of claim 1, wherein the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the second clock signal.

3. (Previously presented) The system of claim 1, wherein the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the third clock signal.

4. (Previously presented) The system of claim 1, further comprising an RC oscillator for generating the second clock signal.

5. (Previously presented) The system of claim 4, wherein the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the third clock signal.

6. (Previously presented) The system of claim 4, wherein the RC oscillator is connected with an external resistor for tuning the second clock signal.

7. (Original) The system of claim 6, wherein the external resistor comprises a variable resistor.

8. (Previously presented) The system of claim 4, wherein the RC oscillator comprises a resistor network for determining the second clock signal.

9. (Currently amended) The system of claim 4, wherein the microprocessor signals the local oscillator to turn off after the ~~packets are~~ digital packet data is transmitted.

10. (Currently amended) The system of claim 4, wherein the converter and transmitter signal the local oscillator to turn off after the ~~packets are~~ digital packet data is transmitted.

11. (Original) The system of claim 1, further comprising a peripheral circuit connected to the microprocessor.

12. (Cancelled).

13. (Original) The system of claim 4, wherein the microprocessor, converter, local oscillator, clock switch, RC oscillator and transmitter are integrated on a chip.

14. (Currently amended) A method for transmitting data with an RF transmitter system having a single crystal oscillator and including a microprocessor connected with a converter that is further in turn connected to a transmitter, the method comprising the steps of:

generating a first clock signal at a radio frequency with a crystal oscillator for providing to the transmitter a carrier signal;

generating a second clock signal and a third clock signal by dividing down the first clock signal for respectively providing to the microprocessor and converter clock signals of respectively reduced frequency;

converting ~~the~~ digital data into digital packet data ~~packets~~ by the converter for output to the transmitter; and

transmitting the ~~packets~~ digital packet data modulated on the first clock signal.

15. (Cancelled).

16. (Currently amended) A method for transmitting data with an RF transmitter system having a single crystal oscillator and including a microprocessor connected with a converter that is in turn connected to a transmitter, the method comprising the steps of:

generating a first clock signal at a radio frequency with a crystal oscillator;

generating a second clock signal using an RC oscillator;

generating a third clock signal from the first clock signal output from the crystal oscillator for coupling to <u>the</u> converter, the third clock frequency being a lower frequency than a frequency of the first clock signal;

generating a fourth clock signal from the second clock signal for coupling to the microprocessor, said fourth clock signal being a lower frequency than the frequency of the first clock signal and being a higher frequency than the third clock signal;

converting <u>digital</u> data output from the microprocessor into ~~packets~~ <u>digital packet data</u> by the converter; and

modulating the ~~packets~~ <u>digital packet data</u> with the first clock signal in the transmitter for transmitting an RF signal therefrom.

17. (Previously presented) The method of claim 16, wherein the step of generating a fourth clock signal from the second clock signal comprises the step of frequency-dividing the second clock signal.

18. (Previously presented) The method of claim 16, further comprising the step of tuning an external resistor connected to the RC oscillator for determining the oscillator output signal.

19. (Previously presented) The method of claim 16, further comprising the step of trimming a built-in resistor network connected to the RC oscillator for determining a frequency of the oscillator output signal.

20. (Previously presented) The method of claim 16, further comprising the step of signaling the crystal oscillator to stop generating the first clock signal after the RF signal is transmitted.

21. (Previously presented) The method of claim 16, further comprising the step of signaling the converter to turn off after the RF signal is transmitted.

22. (Previously presented) The method of claim 16, further comprising the step of signaling the transmitter to turn off after the RF signal is transmitted.